

Summarized Course Description

Course number: ECE 260	Course name: Digital Logic Circuit Design
لغة تدريس المقرر : English	Pre-requisites: MATH 103T
Credit hours: 4 (3-2-0)	Course level: Level - 5

Course Description

وصف المقرر :

Number systems & codes. Logic gates. Boolean algebra. Karnaugh maps. Analysis and synthesis of combinational systems. Decoders, multiplexers, adders and subtractors, PLA's. Types of flip-flops. Memory concept. Counters. Registers. Sequential circuit design. System level digital design. HDL (Verilog) use in the design and synthesis of digital systems. Field-programmable gate arrays (FPGAs).

Course objectives

أهداف المقرر :

1. Introduce digital principle with emphasis on logic design.
2. Familiarize the students with necessary mathematical tools such as number systems, codes, and Boolean algebra .
3. Present the principle of analysis and design of computational logic circuits.
4. Present the principle of analysis and design of sequential logic circuits.

Course Outcomes

مخرجات التعليم:

Upon completing the course, the students will be able to:

1. Understand basic terminology, types of logic gates (AND, OR, NOT, NAND, NOR, XOR)
2. Perform the basic operations used in computers and other digital systems.
3. Apply basic rules of Boolean algebra, De Morgan's laws
4. Utilize the universality of NAND and NOR gates for implementing logic functions.
5. Use Karnaugh maps for circuit minimization.
6. Analyze and design computational logic circuits.
7. Analyze and design sequential logic circuits.
8. Ability to use CAD tools to simulate and verify logic circuits.

Textbook and references

الكتاب المقرر والمراجع المساندة:

Text Book: Digital design by M Morris Mano & Michael D. Ciletti, 5th edition (or later), Pearson; 5 edition (January 9, 2012), ISBN-13: 978-0132774208
ISBN-10: 0132774208

References:

Alan B. Marcovitz, Introduction to Logic Design, third edition, McGraw Hill, 2010
John F. Wakerly, Digital Design: Principles and Practices Package, fifth Edition, Pearson Education, 2017