نموذج (هـ)

Summarized Course Description

Course number: ECE 461	Course name: Digital System Design
لغة تدريس المقرر: English	Pre-requisites: ECE 343
Credit hours: 3 (**3-0-0**)	Course level: Level – 8 or 9

Course Description وصف المقرر :

Design of systems using PLDs and ASICs (in particular, gate arrays and standard cells). Design and implementation details of various systems and logic device technologies. Practical aspects of ASIC design, such as timing, testing, and fault grading. Topics include synchronous design, state machine design, ALU and CPU design, application-specific parallel computer design, design for testability, PALs, FPGAs, VHDL, standard cells, timing analysis, fault vectors, and fault grading.

Course objectives أهداف المقرر :

1. Introduce the concepts and design techniques of Very Large Scale Integration systems through a study of Application Specific Integrated Circuits (ASICs) with particular emphasis on Field Programmable Gate Arrays (FPGAs).

2. Discuss fully custom, standard cell, gate array and programmable ASICs and the influence of total cost on choice of ASIC type.

3. Explore Programmable Logic Devices (PLDs), Field Programmable Gate Arrays (FPGAs). Programming technology. CMOS logic cells. Coarse-grained vs fine-grained architectures. Routing and Timing. I/O cells. Embedded microprocessors.

4. Introduce ASIC Design Software, design flows and design entry methods: Schematic Entry, Hardware Description Languages (HDLs): VHDL.

5. Discuss behavioural and structural models. Event-driven simulation. Logic Synthesis: limitations of HDL based logic synthesis.

Course Outcomes مخرجات التعليم:

On successful completion this course, the student should be able to:

1. Know about the different types of ASIC available and their suitability for different applications.

2. Understand the principles of Programmable ASIC technology.

3. Understand the principles of ASIC design.

4. Describe architecture of FPGAs and their logic and I/O cells. Shows knowledge of timing limitations.

5. Demonstrate understanding of the basic physics of CMOS logic cells. Can build simple logic functions from standard cells.

6. Describe Register Transfer Level (RTL) design: datapath, High Level State Machines (HSM), operator binding, operator scheduling, area-time trade-offs.

7. Perform timing analysis of simple circuits, using reasonable approximations

based on underlying physics.

8. Explain the need for behavioural and structural models for the same circuit. Can perform “dry runs” of VHDL simulations. Can devise simple RTL designs.

9. Describe the limitations and pitfalls of HDL-based logic synthesis and design. Can perform “dry runs” of VHDL simulations showing correct use of Delta Time. Can evaluate alternative RTL designs.

Textbook and references الكتاب المقرر والمراجع المساندة:

Text Book: N. Weste and D. Harris, CMOS VLSI Design: A Circuits and Systems Perspective (4th Edition), 2010. Addison Wesley.

Reference Textbooks:

S.M. Kang and Y. Leblebici, CMOS Digital Integrated Circuits: Analysis and Design (3rd edition), McGraw Hill, ISBN 0-07-246053-9, 2003.

Smith, Douglas. *HDL Chip Design*. Madison, AL: Doone Publishing, 2001. ISBN: 0965193438.

A great book for the intermediate Verilog designer. Clearly outlines the relationship between Verilog models and the corresponding synthesized circuit.

Smith, Michael. *Application-Specific Integrated Circuits*. Reading, MA: Addison Wesley, 1997. ISBN: 0201500221.

A useful reference on many of the lower-level details about synthesis, place and route, and FPGA mapping.

Sweetman, Dominic. *See MIPS Run*. San Francisco, CA: Morgan Kaufman, 1999. ISBN: 1558604103.